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EXAMINER	
MOORE, IAN N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,833	TRAN ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1-16-08* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-4, 6, 8-14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by CS4205 (CyrstalClear Audio Codec '97 product information document).

Regarding Claim 1, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

transmitting audio information segments on a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (OUT, or SDOUT) transmits each audio frame segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs

4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

transmitting a number of synchronization markers (see FIG. 14, transmitting SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being representative of a timing of one of the audio information segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

wherein the audio is communicated devoid of a third signal line (see FIG. on cover page, FIG. 7, Reset# signal line; or SCLK) that carries data different from the audio information segments transmitted on the first signal line (audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from audio information that are transmitted over the SD data line) or

different from the number of synchronization markers transmitted on the second signal line (see FIG. on cover page,7, Reset# signal line; or SCLK audio is transmitted without/devoid the RESET # signal line that carries transmission of commands which are different from pulse

indicating the clock edge transmitted over the SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); note that RESET # signal line is only utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that the system transmits audio without/devoid RESET signal; see page 13 section 2.1; alternatively, see FIG. on cover page; see FIG. 7, 14, SDOUT signal line and LRCLK signal line are sufficient/enough for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that CS4205 is sufficient for communication audio without/devoid SCLK).

Regarding Claim 2, CS4205 Reference discloses the audio comprises a serial bit stream (see page 13, paragraph 2.1; audio stream is a serial bit stream).

Regarding Claim 3, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

Regarding Claim 4, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

Regarding Claim 6, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)).

Regarding Claim 8, CS4205 Reference discloses the format modes are dynamic (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame, thus the audio format/arrangement/layout are dynamic).

Regarding Claim 9, CS4205 Reference discloses the format modes are configured to vary from one information segment to another information segment (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame).

Regarding Claim 10, CS4205 Reference discloses the synchronization marker include sync pulses (see FIG. 14, 17-20; each SYNC/LRCLK pulse; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 11, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 12, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

transmitting audio information segments on a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (IN, or SDI1-3) receives each audio frame segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

receiving audio information segments on a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line (IN&OUT, or SDOUT & SDI1-3), each segment including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

receiving a number of synchronization markers (see FIG. 14, receiving SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being represented of a timing of one of the audio segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

wherein the audio is communicated devoid of a third signal line (see FIG. on cover page, FIG. 7, Reset# signal line; or SCLK) that carries data different from the audio information segments transmitted on the first signal line (audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from audio information that are transmitted over the SD data line) or

different from the number of synchronization markers transmitted on the second signal line (see FIG. on cover page,7, Reset# signal line; or SCLK audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from pulse indicating the clock edge transmitted over the SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); note that RESET # signal line is only utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that the system is sufficient for communication audio without/devoid RESET signal; see page 13 section 2.1; alternatively, see FIG. on cover page; see FIG. 7, 14, SDOUT signal line and LRCLK signal line are sufficient/enough for communicating audio data; note that

SCLK is optional in CS4205, and thus it is clear that CS4205 is sufficient for communication audio without/devoid SCLK).

Regarding Claim 13, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

Regarding Claim 14, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

Regarding Claim 16, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 17, CS4205 Reference discloses a communication system (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system) including a data path (see FIG. 7, 13, SDATA (IN & OUT) line/path, see FIG. 16, SDATA line/path (i.e. SDOUT and SDI 1-3)) configured for transferring audio data (see page 13, paragraph 2,2.1; audio signal) between a transmitting module (see cover page, transmitting unit/module of digital interface/register and/or digital I/O interface/register; FIG. 7, 16, SDATA (OUT); see FIG. 16, SDOUT; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0) and one or more receiving modules (see FIG. on cover page, receiving unit/module of digital interface/register and/or digital I/O

interface/register; FIG. 7, 16, SDATA (IN); see FIG. 16, SDI 1-3; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraphs 6.3-8.0), the transmitting and receiving modules being formed on a printed circuit board (see FIG. on cover page and FIG. 34, transmitting and receive units/modules are inside the CS4205 48-pin integrated circuit on PCB; see page 68-74), the system comprising:

an encoder (see FIG. on cover page; see FIG. 7, 14, Audio Codec with encoding means) positioned within the transmitting module (see FIG. on cover page, encoding is performed in transmitting unit/module of digital interface/register and/or digital I/O interface/register; FIG. 7, 16, encoding is performed in SDATA (OUT); see FIG. 16, encoding is performed in SDOUT; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0) and configured to convert audio data requiring transmission into two-line audio information segments (see FIG. on cover page; FIG. 7, 14, 16-20, converting audio signals into SD data line portions/segments/frames (IN&OUT, or SDOUT & SDI1-3) and SYNC/LRCLK line portions/segments/frames (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

a data line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line portions/segments/frames (IN&OUT, or SDOUT & SDI1-3)) having a first end coupled to a first data port of the encoder (see FIG. on cover page; see FIG. 7, 14, 16-20, SD data interface/port connects/couples to an end/termination point of the SD data line; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0) and configured to transmit the audio information segments (see FIG. 14, 17-20, transmitting audio frame segments/portions/frames, each frame

contains Slots 0-12), the audio information segments (see FIG. 14,17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) including at least an audio format indication (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) including data corresponding to the audio format indication (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes);

a synchronization line (see FIG. 7,14, SYNC/LRCLK line portions/segments (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) having a first end coupled to a second data port encoder (see FIG. on cover page see FIG. 7, 14, 16-20, SYNC/LRCLK data interface/port connects/couples to an end/termination point of the SYNC/CLK line; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0) configured to transmit a number of sync pulses (see FIG. 14, transmitting SYNC pluses; see FIG. 17-20, transmitting LRCLK pluses) each being indicative of a start of one of the audio information segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7); and

a decoder (see FIG. on cover page; see FIG. 7, 14, Audio Codec with decoding means) positioned within the receiving module (see FIG. on cover page, decoding is performed in receiving unit/module of digital interface/register and/or digital I/O interface/register; FIG. 7, 16, decoding is performed in SDATA (IN); see FIG. 16, decoding is performed in SDI1-3; see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0) and having first and second ports respectively coupled to first and second data ports of the decoder (see FIG. on cover page; see FIG. 7, 14, 16-20, end/termination of input/receive interfaces/ports of audio codec with decoding means connect/couple to SD data input/receive interfaces/ports (e.g. SDI1-SDI3); see page 13-14, paragraph 2.1; 2.2; see page 54-57, paragraph 6.3-8.0), the decoder being configured to convert the received two-line audio information segments into audio data (see page 1, 13-21, paragraphs 2-4; page 54-58, paragraphs 6.3-9; audio codec with decoding means decodes/converts/replays the received audio portions/segments/frames into audio data);

wherein the two-line audio information segments (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) are configured to transfer audio data (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

wherein the audio is transferred devoid of a third signal line (see FIG. on cover page, FIG. 7, Reset# signal line; or SCLK) that carries data different from the audio information segments transmitted on the data line (audio is communicated without/devoid the RESET #

signal line that carries transmission of commands which are different from audio information that are transmitted over the SD data line) or

different from the number of sync pulses transmitted on the synchronization line (see FIG. on cover page,7, Reset# signal line; or SCLK audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from pulse indicating the clock edge transmitted over the SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); note that RESET # signal line is only utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that the system is sufficient for communication audio without/devoid RESET signal; see page 13 section 2.1; alternatively, see FIG. on cover page; see FIG. 7, 14, SDOUT signal line and LRCLK signal line are sufficient/enough for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that CS4205 is sufficient for communication audio without/devoid SCLK).

Regarding Claim 18, CS4205 Reference discloses the transmitting and receiving modules are formed on an integrated circuit (see FIG. on cover page and FIG. 34, transmitting and receive units/modules are inside the CS4205 48-pin integrated circuit on PCB; see page 68-74).

Regarding Claim 19, CS4205 Reference discloses wherein the data line is configured for transmitting multi-channel audio data (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; see FIG. on cover page; see FIG. 7, 14, 16-20, 35, SD data line transmits audio frames containing audio channels/slots).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Wolf (US007088398B1).

Regarding Claim 5, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

CS4205 Reference does not explicitly disclose 32 bits. However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the system of CS4205, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

Regarding Claim 15, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags,

command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

CS4205 Reference does not explicitly disclose 32 bits.

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the system of CS4205, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

Regarding Claim 20, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

CS4205 Reference does not explicitly disclose 32 bits. However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the system of CS4205, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Wakazu (US006006287A).

Regarding Claim 7, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)), and transmission of one or more one or more of the transmitted audio segments/frames to an intended recipient (see FIG. 7, controller, see FIG. 16, Stereo DACs) as set forth above in claim 1.

CS4205 Reference does not explicitly disclose audio stream ID includes an indication of an intended recipient.

However, Wakazu teaches the audio stream ID (see FIG. 4, Audio stream ID 2; see FIG. 6, Audio stream IDs A1-A5) includes an indication of an intended recipient of one or more of the transmitted audio segments (see FIG. 2, audio stream ID indicates/identifies the receiver processor 211 or processor 210; see col. 5, line 10 to col. 6, line 60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide audio stream ID includes an indication of an intended recipient, as taught by Wakazu in the system of CS4205, so that it can separate/detect the received data stream according to the stream ID; see Wakazu col. 2, line 10-15, 40-49.

Response to Arguments

6. Applicant's arguments filed claims 1-20 have been fully considered but they are not persuasive.

Regarding claims 1-20, the applicant argued that, "…cited reference fails to disclose or suggest a method for communication audio "wherein the first line and the second line are configured to…..transmitted on the second signal line"…" in page 11-15.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

CS4205 discloses wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

wherein the audio is communicated devoid of a third signal line (see FIG. on cover page, 7, Reset# signal line; or SCLK) that carries data different from the audio information segments transmitted on the first signal line (audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from audio information that are transmitted over the SD data line) or

different from the number of synchronization markers transmitted on the second signal line (see FIG. on cover page,7, Reset# signal line; or SCLK audio is communicated without/devoid the RESET # signal line that carries transmission of commands which are different from pulse indicating the clock edge transmitted over the SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); note that RESET # signal line is only utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data.

Thus, it is clear that the system is sufficient for communication audio without/devoid RESET signal; see page 13 section 2.1; alternatively, see FIG. on cover page; see FIG. 7, 14, SDOUT signal line and LRCLK signal line are sufficient/enough for communicating audio data; note that SCLK is optional in CS4205, and thus it is clear that CS4205 is sufficient for communication audio without/devoid SCLK).

Regarding claims 1-20, the applicant argued that, "...interface between CS4205 and DC'97 controller at least three of these wires carrying different data are necessary...BIT CLK...SYNC...SDATA OUT/SDATA IN; the interface between CS4205 and stereo DAC at least three signals are necessary...SCLK/MCLK, LRCLK, SDOUT; the interface between CS4205 and stereo ADC three lines are still necessary SCLK/MCLK, LRCLK, SDI1/SDI2/SDI3..." pages 11-15.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Applicant argument is based on incorrectly counting every possible connection, and where the claim invention recites "transmitting....on a first signal line", "transmitting...on a second signal line", and the claimed invention shown in FIG. 1-2, transmitter transmitting first signal line and second signal line. Thus, examiner is asserting the applicant claimed invention in light of the specification, the first signal line as transmitting SD data line (OUT, or SDOUT) and the second signal line as transmitting SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ian N. Moore
Examiner
Art Unit 2616

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